Patent claims

1. A method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps,
wherein
a) the data are read from a memory (1) organized on a page-for-page basis,
b) the intermediate step prescribed by the transform is carried out,
c) the resulting data are stored in a buffer memory (5), and
d) the resulting data are written page-for-page from the buffer memory (5) to the memory (1) organized on a page-for-page basis.

2. A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,
wherein
a) the data are read from a memory (1) organized on a page-for-page basis,
b) the data are stored in a buffer memory (5),
c) the intermediate step prescribed by the transform is carried out, and
d) the resulting data are written page-for-page to the memory (1) organized on a page-for-page basis.

3. A method for calculating an orthogonal discrete transform in prescribed intermediate steps,
wherein
the data are read from two memories (3, 4) organized on a page-for-page basis such that the reading is organized on a page-for-page basis,
the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories (3, 4) organized on a page-for-page basis.

4. The method as claimed in one of claims 1 to 3, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

5. The method as claimed in claim 4, wherein the transform has an identical geometry for each stage.

6. The method as claimed in claim 5, wherein an FFT or IFFT based on Singleton is used.

7. An apparatus for carrying out the method as claimed in one of claims 1, 4-6,
wherein
the apparatus has a memory (1) organized on a page-for-page basis, a processor (2) and a directly organized memory (5) which is arranged downstream of the processor.

8. An apparatus for carrying out the method as claimed in one of claims 2, 4-6,
wherein
the apparatus has a memory (1) organized on a page-for-page basis, a processor (2) and a directly organized buffer memory (5) which is arranged upstream of the processor.

9. The apparatus as claimed in one of claims 7 or 8, wherein the page-oriented memory (1) is a large memory in relation to the directly organized buffer memory (5).

10. The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory (5).

11. The apparatus as claimed in one of claims 7-10, wherein the page-oriented memory (1) is a DRAM and the buffer memory (5) is an SRAM.

12. The apparatus as claimed in one of claims 7 - 11, wherein the page-oriented memory (1) has a size of 8 K addresses and the buffer memory (5) has a size of 32 - 64 addresses.

13. An apparatus for carrying out the method as claimed in one of claims 3, 4-6,
wherein
the apparatus has two memories (3, 4) organized on a page-for-page basis and a processor (2).

14. The apparatus as claimed in claim 13, wherein the page-oriented memories (3, 4) are of the same size.

15. The apparatus as claimed in claim 14, wherein the page-oriented memory (3, 4) has a size of 4 K addresses.

16. The apparatus as claimed in one of claims 7 - 15, wherein the processor (2) provides a Butterfly.